Remarks

This is in response to the final Office Action mailed September 13, 2006, which rejected pending claims 1-20. The Applicant respectfully requests reconsideration of this final rejection of the claims.

Rejection of Claims Under 35 U.S.C. §102(e)

Claims 1-2, 6-7 and 19-20 were rejected as being anticipated by U.S. Published Patent Application No. US2004/0019776 to Sato et al. ("Sato '776") on the basis that the spindle motor 104 of Sato '776 was viewed as not being under processor control during the boot process. This characterization of Sato '776 is respectfully traversed.

The disk controlling section 411 is described by Sato '776 as operating to exchange control data between the processor 412 and the spindle motor 404. (*"A disk controlling section 411 intermediates exchange of control data on the operation of a hardware section between a processor 412 and the hardware section..."* Sato '776, para. [0006], lines 1-7). The phrase "exchange of control data" indicates to the skilled artisan that the disk controlling section 411 is a conduit to enact commands by the processor 412 (e.g., accelerate the motor 404) and to report back to the processor ongoing status data (e.g., present speed of the motor 404) during processor control of the hardware section.

It is in this context that Sato '776 describes the operation of the processor 412 and the disk controlling section 411 during the boot process of FIG. 5. The processor 412 provides commands to the disk controlling section 411, such as to accelerate the motor at step 301 and to carry out a seek operation at step 303. In response, the disk controlling section 411 provides status data back to the processor 412 during execution of the

commands, such as indicated by decision steps 302 and 304. These continuous and ongoing exchanges between the processor 412 and disk controlling section 411 would not be viewed by the skilled artisan as an "open control mode," as claimed.

The Examiner relies upon a definition of "open control mode" provided in the specification at page 16 lines 16-21 in support of the view that the disk controlling section 411 operates apart from the processor 412. Such reliance is respectfully misplaced.

The definition of "open control mode" provided in the specification does not merely describe a mode of operation "*whereby the electrical load continues to operate using settings established by the processor.*" If this is all that the specification stated, the Examiner might have a valid point since Sato '776 makes it clear that the disk controlling section 411 operates in response to a "setting" (e.g. a commanded speed) provided by the processor 412.

However, the text more fully states, "*whereby the electrical load continues to operate using settings established by the processor prior to the release of processor control and without further processor regulation or intervention.*"

The skilled artisan would understand "release of processor control" to be an affirmative step that must be carried out before the "open control mode" can be enacted. See e.g., present application, step 3 in FIG. 8; step 258 in FIG. 9. Merely commanding a setting does not invoke "open control mode" unless processor control is also released.

Since Sato '776 explicitly provides continuous exchange of control data between the processor 412 and the disk controlling section 411, no such release of processor control takes place. Rather, the skilled artisan would view the electrical loads in Sato '776 to be under continuous processor control during the boot process.

Accordingly, there is nothing in Sato '776 that explicitly or inherently discloses a step of *"releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code"* as recited by claim 1. Reconsideration and withdrawal of the rejection of claim 1, and for the claims depending therefrom, are respectfully requested on this basis.

Rejection of Claims Under 35 U.S.C. §103(a)

Claims 3-5 and 8-18 were rejected as being obvious over Sato '776 in view of U.S. Patent No. 6,405,311 to Broyles et al. ("Broyles '311"). This rejection is respectfully traversed.

Both Sato '776 and Broyles '311 are silent with regard to teaching or suggesting a step of *"continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location,"* as featured by independent claim 8.

It appears that the Examiner has found that from the time that the processor 412 commands a first target speed for the motor (5400 RPM) until the time that the processor 412 commands a second, higher target speed for the motor (e.g. 15,000 RPM), the processor enters a period of suspended processor operational control. See final Office Action, page 8, lines 2-3; Sato '776, paras [0085] and [0089]. This is believed to be an erroneous characterization of the reference.

As pointed out above, Sato '776 does not describe any type of temporary suspension of processor control in this intervening period. In steps 301 and 302 of FIG. 5, the processor 412 commands the first speed (5400 RPM) and then receives continuous

feedback from the disk controlling section 411 as to the present speed of the motor. This feedback is used to allow the processor 412 to decide when it is time to proceed with the next step in the process, i.e., moving the head to the appropriate destination to retrieve the main program from the disc at step 303.

It is incontrovertible that the disk controlling section 411 sends speed control data to the processor 412 during steps 301 and 302. There is further nothing that teaches or suggests that the disk controlling section 411 stops sending this speed control data to the processor 412 once step 302 in the routine is completed. Rather, the skilled artisan would clearly view this data as being continuously provided by the section 411 to the processor 412 for use in the processor's top level control for the entire storage system.

For example, it is wholly implausible to assert that the processor 412 would be oblivious to a failure of the motor 404 during the boot process, and yet this is the position that the Examiner has taken in suggesting that processor control is suspended during this interval.

It is further implausible to assert that the disk controlling section 411, after having stopped sending speed control data to the processor during steps 303 through 307 of the routine of FIG. 5 as asserted by the Examiner, suddenly begins sending it again to the processor 412 for use in steps 308, 309 and 310 of FIG. 5 to verify the speed of the motor 404 and, if necessary, increase it to the final operational speed. Para [0089] and [0090].

Claim 8 affirmatively requires "*processor operational control of the electrical load is temporarily suspended.*" As with the phrase "open control mode," the Applicant provides a definition of "operational control" as including *"a mode of operation whereby the processor engages in continual active regulation, intervention or verification to*

maintain the continued operation of the load, or simply a mode where the processor controls the load." Specification, p. 16, lines 22-25.

The Applicant respectfully submits that the Examiner has not shown, and cannot show, a teaching or suggestion in Sato '776 where such operational control is temporarily suspended, as claimed.

Indeed, the Examiner's construction of "operational control" as being limited to just those points in time when a command is being issued is improper as being contrary to the above definition, since the definition covers periods of time in which a command has been issued and then feedback is provided to monitor the ongoing execution of that command (as with the disk controlling section 411 of Sato '776).

Accordingly, the Applicant submits that Sato '776 and Broyles '311, alone or in combination, fail to teach or suggest all of the limitations set forth by claim 8. Moreover, there is nothing that would motivate one skilled in the art to combine/modify these references to arrive at the subject matter of claim 8. Reconsideration and withdrawal of the rejection of claim 8, and for the claims depending therefrom, are requested on these bases.

For similar reasons, the cited references fail to teach or suggest a programmable processor that "*temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location, and resumes operational control of the electrical load using the application code*" as recited by independent claim 15. Reconsideration and withdrawal of the rejection of claim 15, and for the claims depending therefrom, are also requested for the foregoing reasons.

RECEIVED
CENTRAL FAX CENTER
NOV 27 2006

Conclusion

The Applicant respectfully requests reconsideration and allowance of all of the claims pending in the application. This Response is intended to be a complete response to the final Office Action mailed September 13, 2006. Should any questions arise concerning this response, the Examiner is invited to contact the below signed Attorney.

Respectfully submitted,

By: _____

Randall K. McCarthy, Registration No. 39,297
Mitchell K. McCarthy, Registration No. 38,794
Fellers, Snider, Blankenship, Bailey and Tippens
100 N. Broadway, Suite 1700
Oklahoma City, Oklahoma 73102
Telephone: (405) 232-0621
Facsimile: (405) 232-9659
Customer No. 33900